Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] An integrated circuit (IC) comprising:
an FET transistor having a gate disposed between a source and a drain;
a gate dielectric layer disposed underneath the gate; and
a spacer on a side of the gate, wherein
the gate dielectric layer is oxide; and the spacer has a reduced dielectric constant (k).

[c2] The IC, according to claim 1, wherein the reduced dielectric constant (k) is less than 3.85.

[c3] The IC, according to claim 1, wherein the reduced dielectric constant (k) is less than 7.0, but greater than 3.85.

[c4] The IC, according to claim 1, wherein the spacer comprises a material which can be etched selectively to the gate dielectric layer.

[c5] The IC, according to claim 1, wherein the spacer is porous, and further comprising a thin layer deposited on the spacer to prevent moisture absorption.

[c6] The IC, according to claim 5, wherein the thin layer com-

prises oxide.

[c7] The IC, according to claim 5, wherein the thin layer has a thickness of less than 5 nm.

[c8] The IC, according to claim 5, wherein the thin layer has a thickness of approximately 1-2 nm.

[c9] The IC, according to claim 1, wherein the spacer comprises a material selected from the group consisting of Black Diamond, Coral, TERA and Blok type materials.

[c10] A method of forming a spacer for a gate electrode of a transistor comprising the steps:
depositing a dielectric material;
etching the dielectric material to form a spacer;
forming pores in the dielectric material; and
depositing a thin layer over the porous dielectric material.

[c11] The method, according to claim 10, wherein the spacer is made porous by exposing the spacers to an oxygen plasma.

[c12] The method, according to claim 10, wherein:
the spacer comprises organic material; and
the spacer is made porous by removing the organic material.

[c13] The method, according to claim 10, wherein the spacer comprises a Si-O-C-N type of low-k material.

[c14] The method, according to claim 10, wherein the pores are formed during the spacer etch, rather than during deposition of the dielectric material.

[c15] The method, according to claim 10, wherein the spacer has a reduced dielectric constant (k).

[c16] The method, according to claim 15, wherein the reduced dielectric constant (k) is less than 3.85.

[c17] The method, according to claim 15, wherein the reduced dielectric constant (k) is less than 7.0, but greater than 3.85.

[c18] The method, according to claim 15, wherein the spacer is porous, and further comprising depositing a thin layer on the spacer to prevent moisture absorption.

[c19] The method, according to claim 10, wherein the thin layer comprises oxide.

[c20] The method, according to claim 10, wherein the thin layer has a thickness of less than 5 nm.